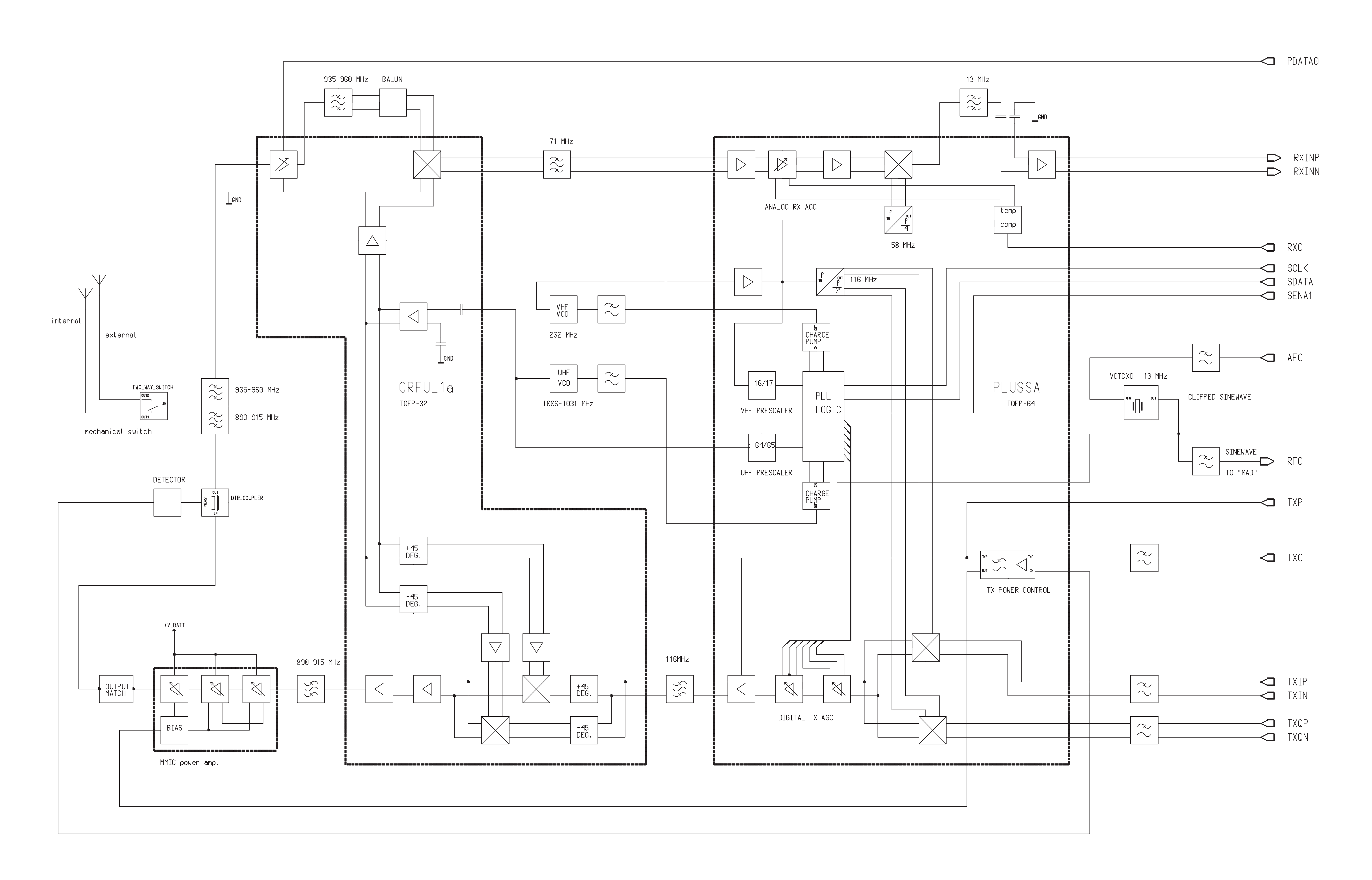
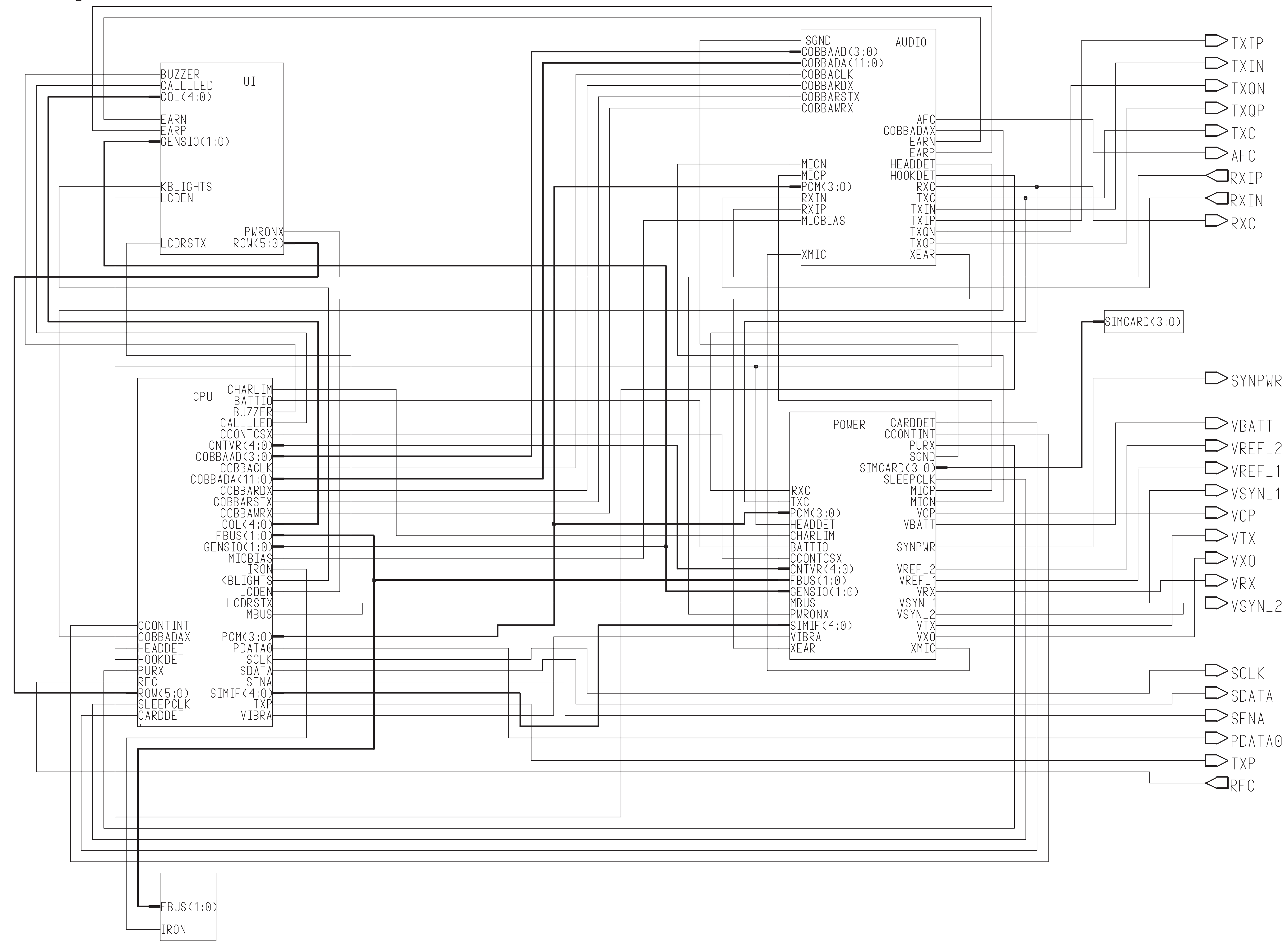
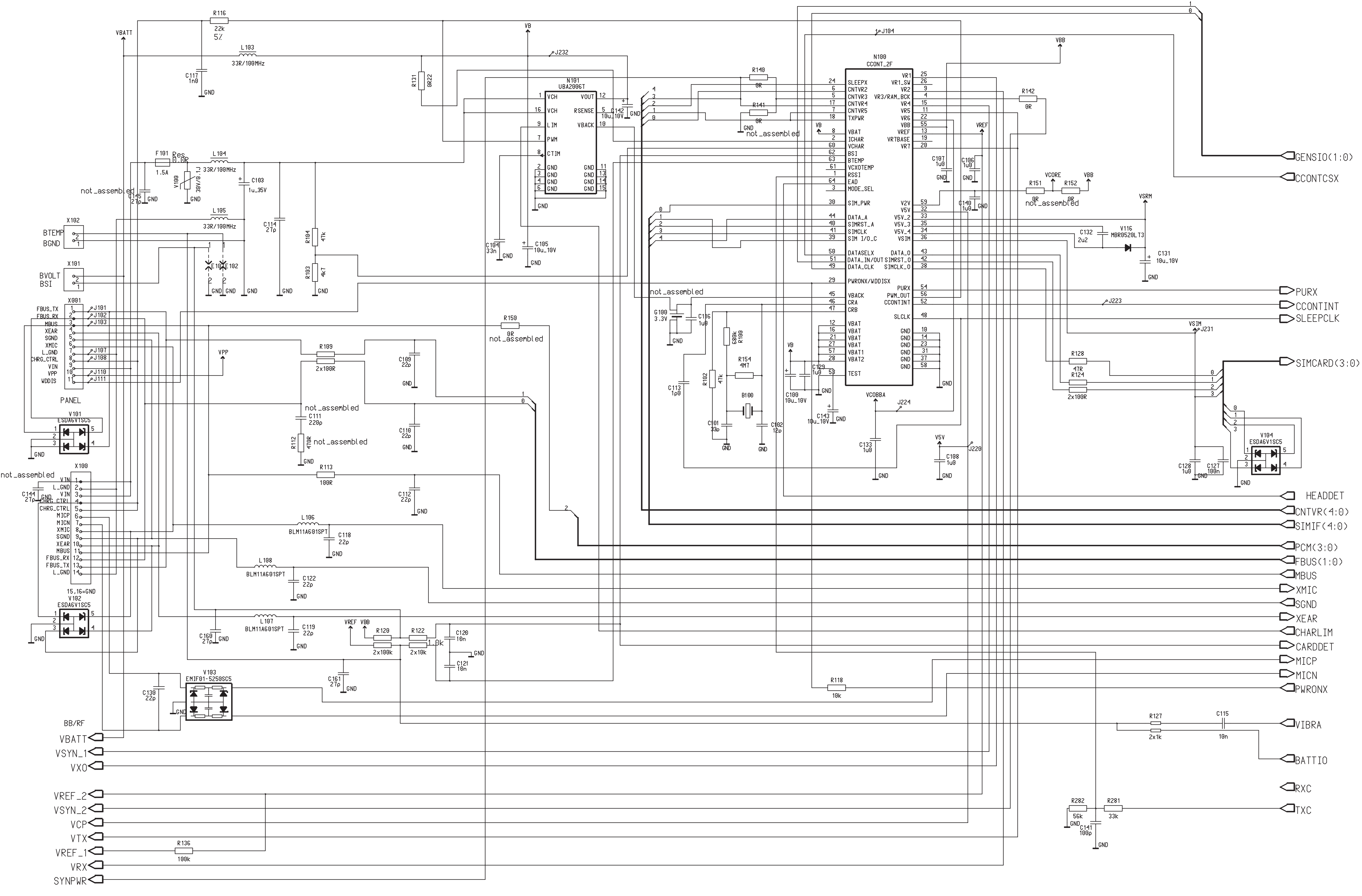
Block Diagram of System/RF Blocks



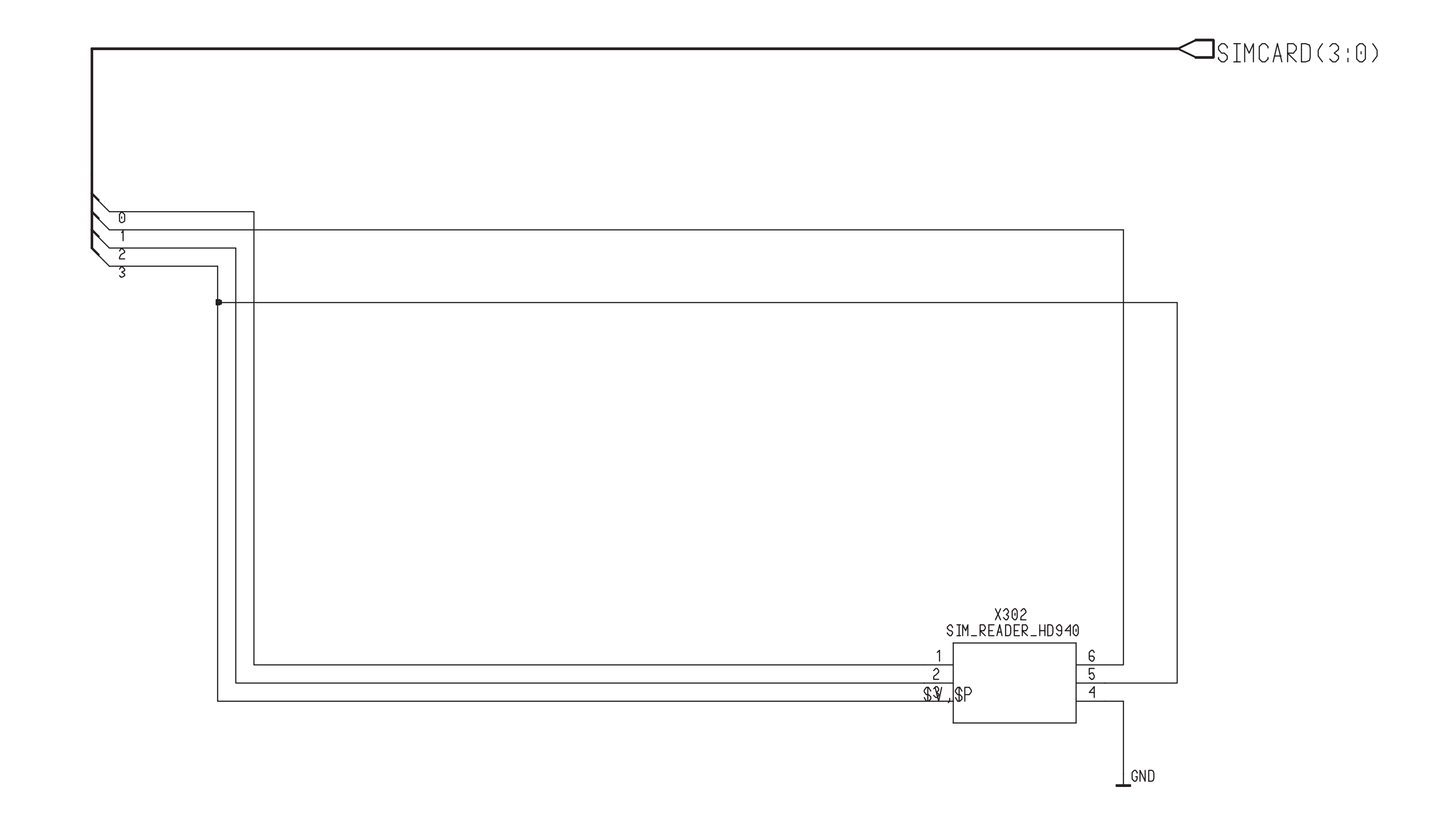
Circuit Diagram of Baseband (Version 12 Edit 8) for layout version 14



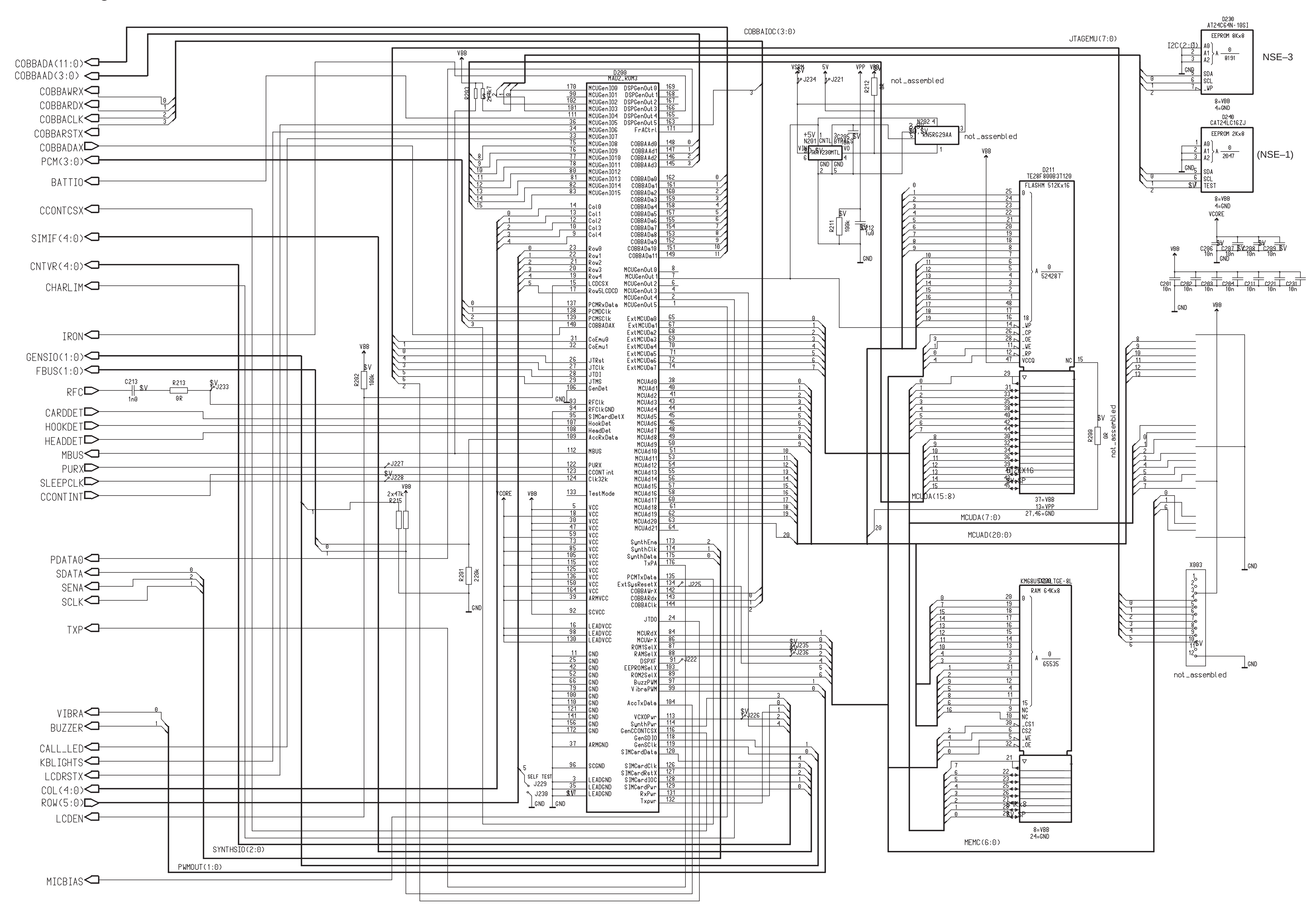
Circuit Diagram of Power Supply (Version 14 Edit 41) for layout version 14



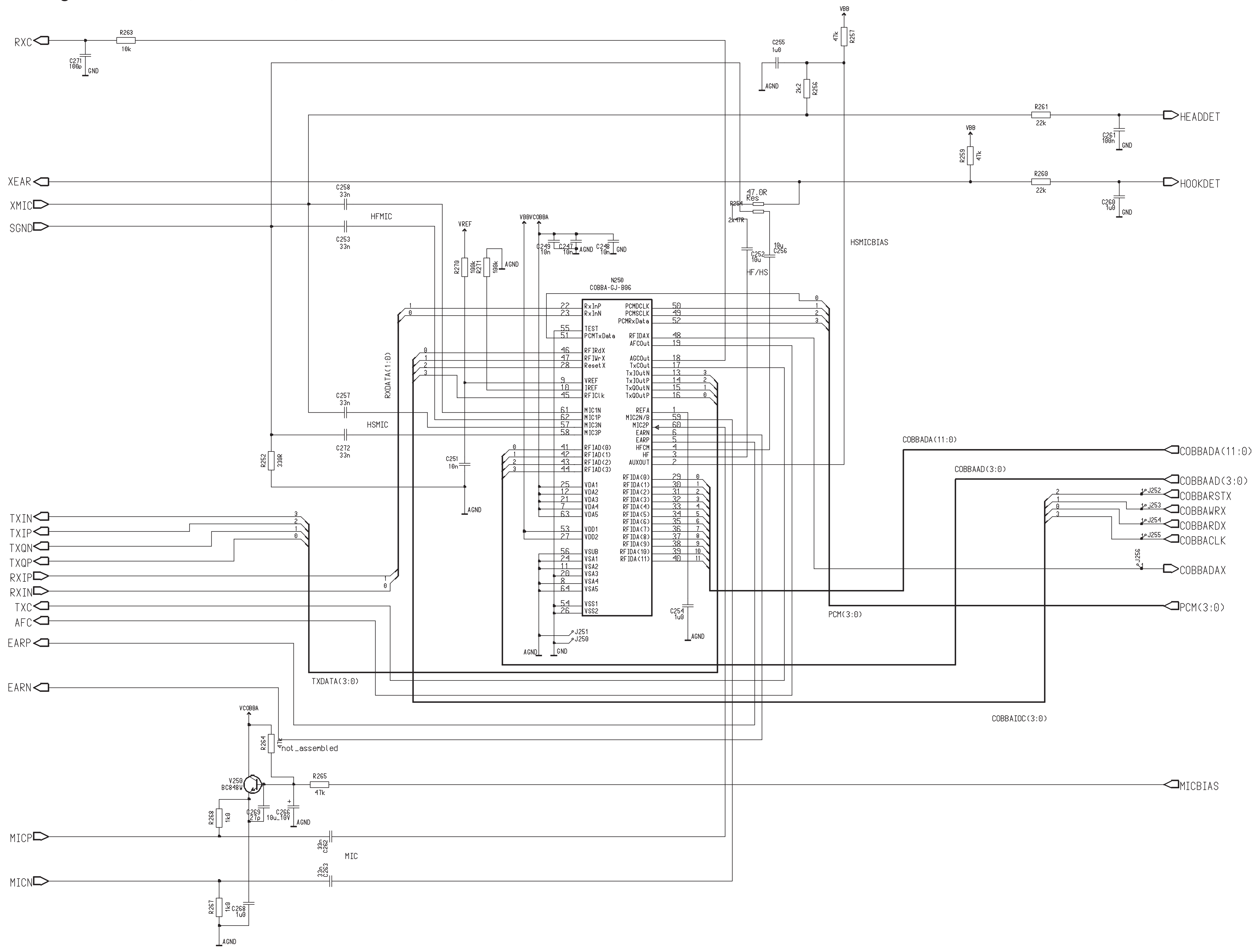
Circuit Diagram of SIM Connectors (Version 14 Edit 9) for layout version 14



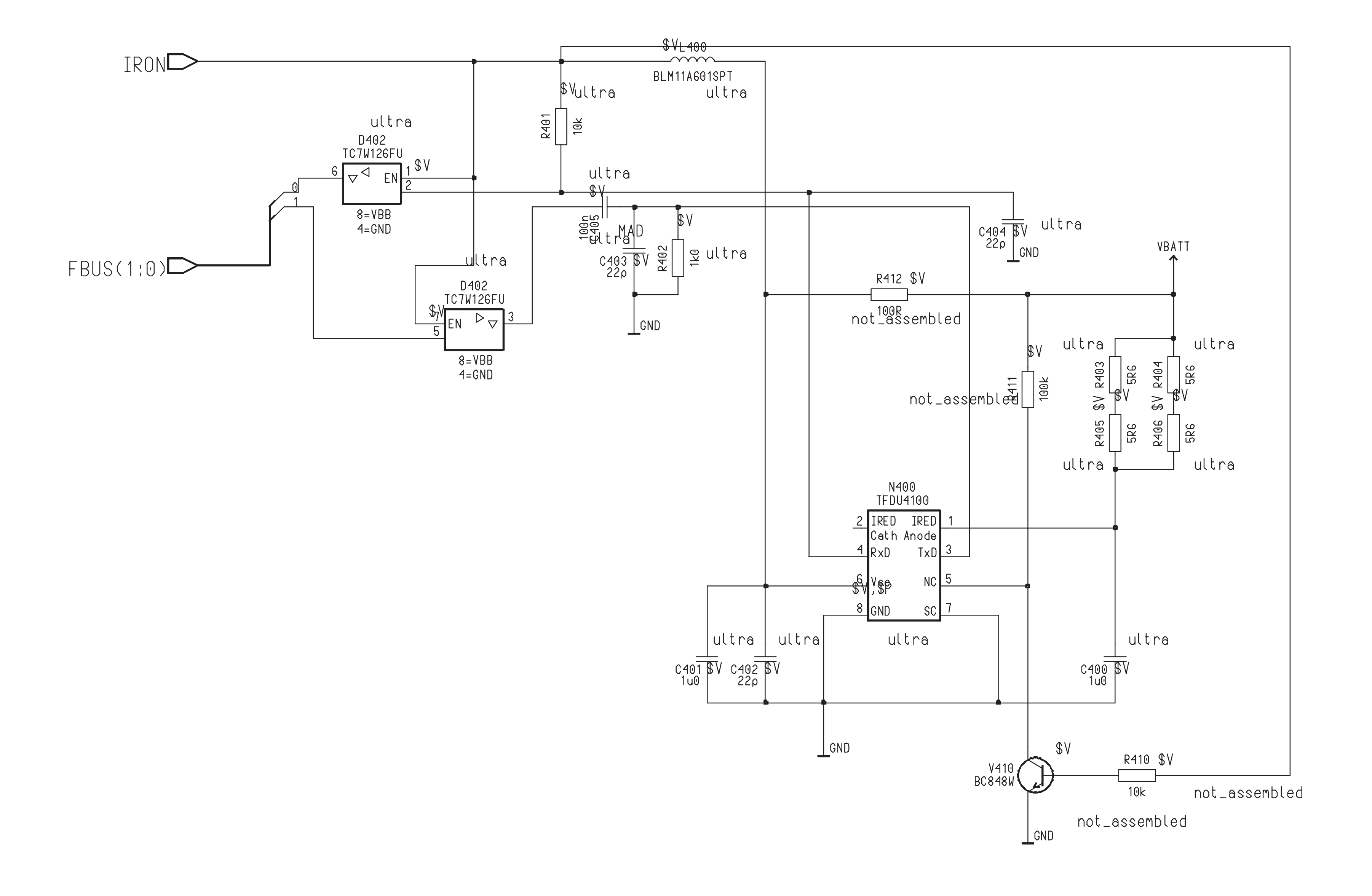
Circuit Diagram of CPU Block (Version 14 Edit 23) for layout version 14



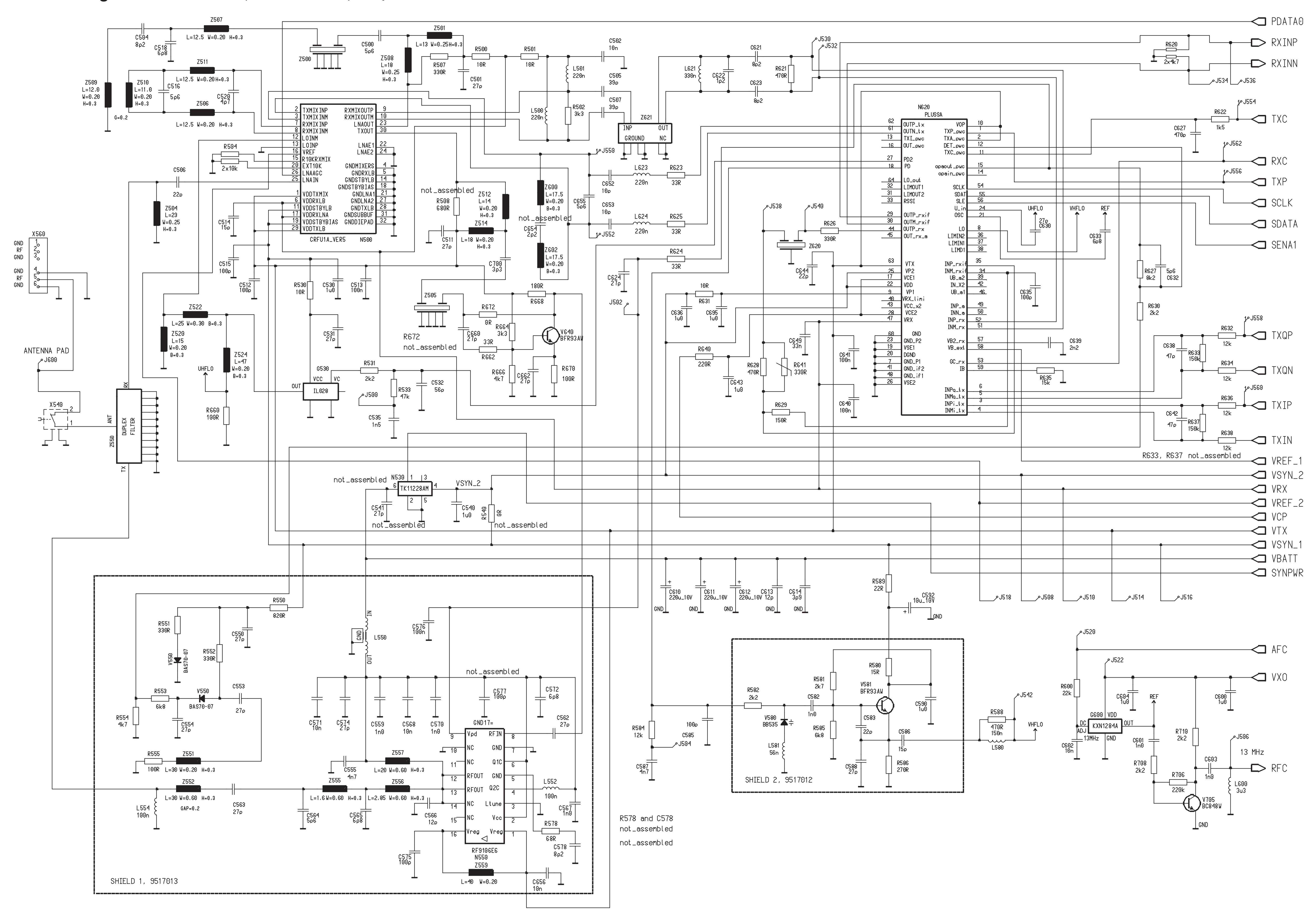
Circuit Diagram of Audio (Version 14 Edit 27) for layout version 14



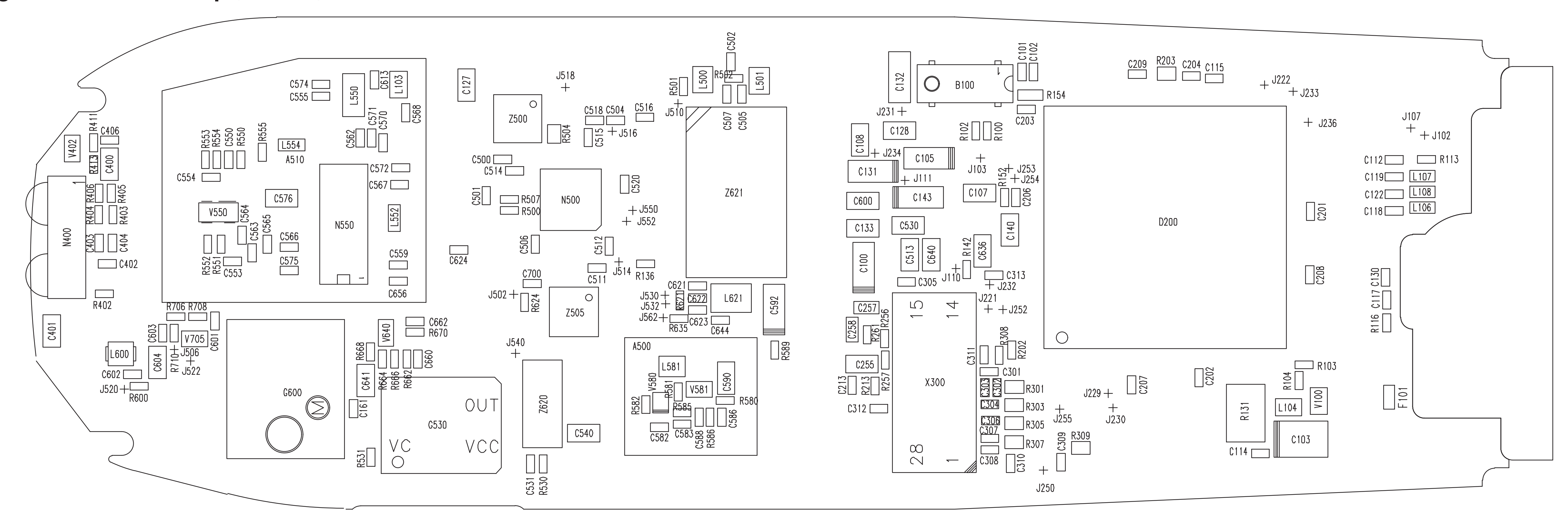
Circuit Diagram of IR Module (Version 14 Edit 21) for layout version 14



Circuit Diagram of RF Block (Version 14 Edit 26) for layout version 14



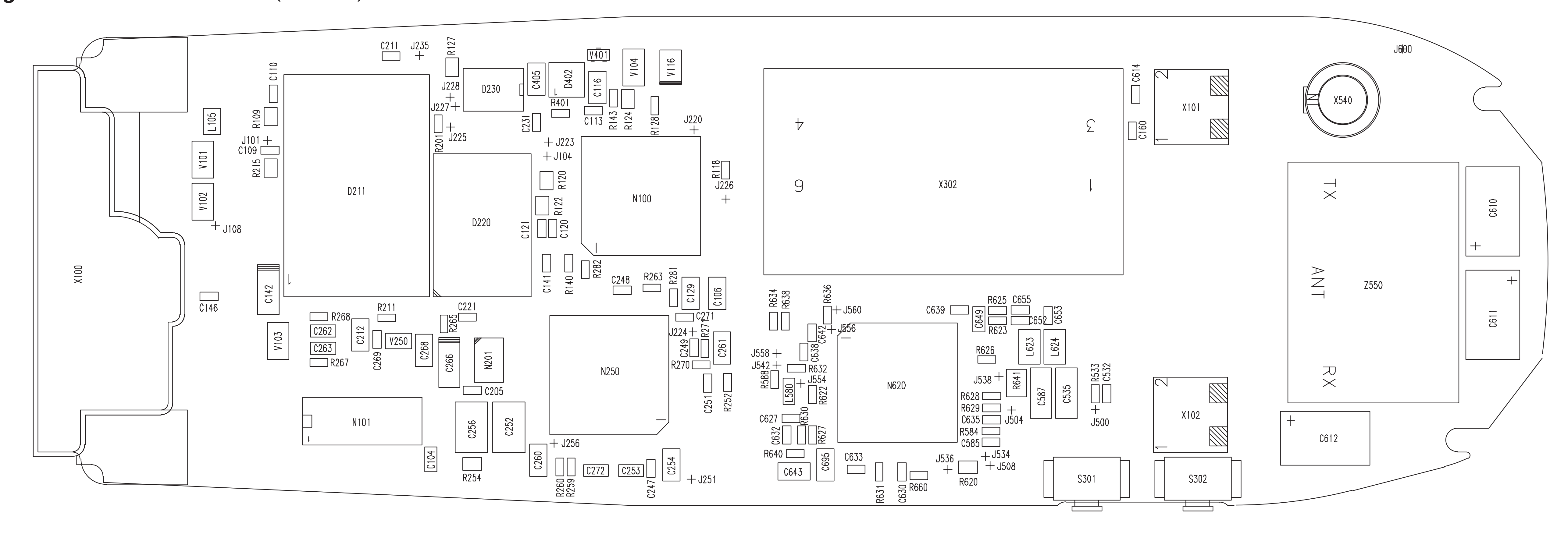
Layout Diagram of UPT8T – Top (Version 14)



testpoint	name	condition	dc–level	ac–level
J102	FBUS_RX	power on	pulsed DC (0V/2.8V)	
J103	MBUS	power on	pulsed DC (0V/2.8V)	
J107	LGND		0V	
J110	VPP	flash programming	nominal 5V (5V flash) or 3.0V (3V flash)	
J111	WDDISX	power on	reset state 0V, normal state 2.8V	
J221	5V	flash programming	nominal 5.0V (5V flash) or 3.0V (3V flash)	
J222	DSPXF	power on	pulse active 0V, non–active 2.8V	
J229	MAD selftest	test mode set externally		
J230	MAD selftest	test mode set externally		
J231	VSIM	SIM power on	nominal 2.8V (3V SIM card) or 5.0V (5V SIM card)	
J232	VB (battery voltage in baseband)	battery connected	nominal 3.6V (min 3.0, max 4.2)	
J233	RFCLK	active state		typ. 1.0Vpp (min 0.5Vpp, max 2.0Vpp)
J234	VSRM	power on	nominal 5.5V (min 5V, max 6V)	CCONT switch mode regulator ripple voltage
J236	RAMSELX	active state	pulse active 0V, non–active 2.8V	
J250	GND		0V	
J252	COBBARSTX	power on	reset state 0V, normal state 2.8V	
J253	COBBAWRX	active state	pulse active 0V, non–active 2.8V	
J254	COBBARDX	active state	pulse active 0V, non–active 2.8V	
J255	COBBACLK	active state	pulsed DC (0V/2.8V)	

testpoint	name	condition	dc–level	ac–level
J502	Power control op.amp output voltage to N550 (Vpd, pin)	power level depended	pulsed DC	
J506	RFC (13 MHz sine-wave)		0 V	typ. 1.0 Vpp min 0.5/max 2.0 Vpp
J510	VRX (regulated supply for RX)		2.8 V min 2.7 / max 2.85 V, pulsed	
J514	VTX (regulated supply for TX)		2.8 V min 2.7 / max 2.85 V, pulsed	
J516	VSYN_1 (regulated supply for VCOs)		2.8 V min 2.7 / max 2.85 V	
J518	VREF_2 (ref. voltage for N500)		1.5 V +/– 1.5%	
J520	AFC (autom. freq. cntrl)		0 – 2.3 V, typ. 1.15 V (room temp.)	
J522	VXO (regulated supply for VCTCXO)		2.8 V min 2.7 / max 2.85 V	
J530 & J532	71 MHz IF input to N620	–95 dBm @ X540 (ext. RF connector)	typ. ca. 1.2 V pulsed	typ 100 – 140 uVpp balanced voltage at 71 MHz
J540	13 MHz output from N620 to Z620	–95 dBm @ X540 (ext. RF connector) RXC at level of full calibrated gain	typ. ca. 1.5 V pulsed	typ. ca. 700 uVrms
J550 & J552	116 MHz TX IF to N500		typ. ca. 1.1 – 1.2 V pulsed	typ. ca. 100 mVrms each
J562	RXC (receive gain control voltage)	RX gain setting depended	control range is 0.5 – 1.45 V, ,pulsed. typ. 1.3–1.4 V for calibrated maximum gain	

Layout Diagram of UPT8T – Bottom (Version 14)



testpoint	name	condition	dc–level	ac–level
J101	FBUS_TX	active state	pulsed DC (0V72.8V)	
J104	CCONTCSX (CCONT chip select)	active state	pulse active 0V, non–active 2.8V	
J108	CHRG_CTRL	charger connected	pulsed DC (0V/2.8V)	
J220	V5V	active state	nominal 5.0V (min 4.8V, max 5.2V)	
J223	CCONTINT (charger, RTC interrupt)	interrupt	pulse active 2.8V, non–active 0V	
J224	VCOBBA	active state	nominal 2.8V (min 2.7V, max 2.85V)	
J225	EXTSYSRESETX	power on	reset state 0V, normal state 2.8V	
J226	VCXOPWR	power on	active state 2.8V, non–active 0V	
J227	PURX (power on reset)	power up/down	reset state 0V, normal state 2.8V	
J228	SLEEPCLK (32kHz clock)	power on	pulsed DC (0V/2.8V)	
J235	ROM1SELX	active state	pulse active 0V, non–active 2.8V	
J251	AGND	pcb ground	0V	
J256	COBBADAX	active state	pulse active 0V, non–active 2.8V	

testpoint	name	condition	dc–level	ac–level
J500	Control voltage for UHF VCO module G600	channel 60 channel 1 channel 124	2.25 +/– 0.25 V > 0.8 V < 3.7 V	
J504	Control voltage for VHF VCO circuit		typ. 2.0 –2.2 V min 0.5 / max 4.0 V	
J508	VSYN_2 (regulated supply for PLLS)		2.8 V min 2.7 / max 2.85 V	
J534&J536	13 MHz IF output to N250	–95 dBm @ X540 (ext. RF connector) RXC at level of full calibrated gain	typ ca. 1.0 – 1.1 V pulsed min. 0.7 / max. 1.4 V	typ. 50 mVpp balanced voltage at 13 MHz
J538	13 MHz output from Z620 to N620	–95 dBm @ X540 (ext. RF connector) RXC at level of full calibrated gain	typ. ca. 1.5 V pulsed	typ. ca 600 uVrms
J542	VHF VCO output (232 MHz)		–	typ. 400 mVpp. > 100 mVpp required
J554	TXC (TX power control voltage)		@level 19 typ. ca. 0.6 V pulse @level 5 typ ca. 1.8 V pulse	
J556	TXP (TX enable)		2.8 V logic level pulse, (max. 0.8 V ”0” / min 2.0 V ”1”)	
J558	TXQP (other half of balanced Q–signal)		0.8 V pulsed	400 mVpp
J560	TXIP (other half of balanced I–signal)		0.8 V pulsed	400 mVpp